

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	12225	SDRAM or (synchronous adj dynamic adj random adj access adj memory)	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:46
L2	2005	row adj address adj decoder	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:46
L3	1863	column adj address adj decoder	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:47
L4	5706	mode adj register	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:47
L5	2	transparent adj memory adj array	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:49
L6	114	transparent adj memory	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:48
L7	15	1 and 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:49
L8	1387	2 and 3	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:48
L9	1	6 and 8	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:48
L10	10	4 and 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:52

L11	1	2 and 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:49
L12	1	3 and 6	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:49
L13	4889	synchronous adj DRAM	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:52
L14	0	6 same 13	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:52
L15	5	6 and 13	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 19:55
L16	2	(("6260127") or ("5825704")). PN.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:04
L17	1280	(711/167).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:06
L18	506	(711/168).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:06
L19	528	(711/169).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:06
L20	1415	(711/170).CCLS.	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:21
L21	322	embedded same SDRAM	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:21

L22	125	embedded with SDRAM	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:22
L23	28	22 same controller	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:23
L24	15	transparent with SDRAM	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:23
L25	67	transparent same SDRAM	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:23
L26	46	21 and transparent	US-PGPU B; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/11 20:23